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G. Dröge , M. Thole , E.-H. Horneber

**Proceedings of the conference on Design, automation and test in Europe** February 1998

The EASY analog design system includes a qualitative analysis tool for examination of the principal aptitude of a chosen circuit structure, as well as a symbolic analysis component. It allows the deduction of compact but sufficiently accurate design equations. These tools support the first steps of the design process and give insight in the behavior of the analog circuit.

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**1 BRASIL: the Braunschweig mixed-mode-simulator for integrated circuits**

*Bretthauer, U.; Horneber, E.-H.;*  
Design Automation Conference, 1996, with EURO-VHDL '96 and  
Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sept. 1996  
Page(s): 10 -14

[\[Abstract\]](#) [\[PDF Full-Text \(472 KB\)\]](#) **IEEE CNF**

**2 Detection of critical hazards in digital MOS VLSI circuits by switch-level timing simulation**

*Sass, D.; Warmers, H.; Horneber, E.-H.;*  
Circuits and Systems, 1990., Proceedings of the 33rd Midwest  
Symposium on , 12-14 Aug. 1990  
Page(s): 584 -587 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(228 KB\)\]](#) **IEEE CNF**

**3 Switch-level timing models in the MOS simulator BRASIL**

*Warmers, H.; Sass, D.; Horneber, E.-H.;*  
Design Automation Conference, 1990. EDAC. Proceedings of the  
European , 12-15 March 1990  
Page(s): 568 -572

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A. Papanikolaou , M. Miranda , F. Catthoor , H. Corporaal , H. De Man , D. De Roest , M. Stucchi , Karen Maex

**Proceedings of the 2003 international workshop on System-level interconnect prediction**  
April 2003

In this paper we show how to exploit energy-delay trade-offs that exist due to the variation of the technology parameters for the implementation of interconnect wires. We also evaluate how these trade-offs can be propagated to the memory module level, so we can minimise the power consumption of the entire memory organisation (i.e., memories and connections between them). Our approach is that at future technology nodes the delay problem can be handled at the application level, so given any delay ...

2 [Energy-performance trade-offs for spatial access methods on memory-resident data](#) 80%

Ning An , Sudhanva Gurumurthi , Anand Sivasubramaniam , Narayanan Vijaykrishnan , Mahmut Kandemir , Mary Jane Irwin

**The VLDB Journal &mdash; The International Journal on Very Large Data Bases**  
November 2002

Volume 11 Issue 3

The proliferation of mobile and pervasive computing devices has brought energy constraints into the limelight. Energy-conscious design is important at all levels of system architecture, and the software has a key role to play in conserving battery energy on these devices. With the increasing popularity of spatial database applications, and their anticipated deployment on mobile devices (such as road atlases and GPS-based applications), it is critical to examine the energy implications of spatial ...

3 [An O\(n\) algorithm for transistor stacking with performance constraints](#) 80%

Bulent Basaran , Rob A. Rutenbar

**Proceedings of the 33rd annual conference on Design automation conference** June 1996

4 ASIC design in nanometer era - dead or alive?: Designing mega-ASICs in nanogate technologies 77%  
A David E. Lackey , Paul S. Zuchowski , Juergen Koehl  
**Proceedings of the 40th conference on Design automation** June 2003  
This paper discusses challenges the designer faces in integrating entire system product designs, containing tens or even hundreds of millions of logic gates, into single chip solutions now within reach using circuit densities possible in the latest silicon technologies. Managing designs of this size presents a new dimension of issues, and managing the physical and electrical effects of these high density device geometries presents another; solutions in both these areas are presented.  
Lastly, thi ...

5 JouleTrack: a web based tool for software energy profiling 77%  
A Amit Sinha , Anantha P. Chandrakasan  
**Proceedings of the 38th conference on Design automation** June 2001  
A software energy estimation methodology is presented that avoids explicit characterization of instruction energy consumption and pre-dicts energy consumption to within 3% accuracy for a set of bench-mark programs evaluated on the StrongARM SA-1100 and Hitachi SH-4 microprocessors. The tool, JouleTrack, is available as an online resource and has various estimation levels. It also isolates the switch-ing and leakage components of the energy consumption.

6 Preservation of passivity during RLC network reduction via split congruence transformations 77%  
A Kevin J. Kerns , Andrew T. Yang  
**Proceedings of the 34th annual conference on Design automation conference** June 1997

7 BRASIL: the Braunschweig mixed-mode-simulator for integrated circuits 77%  
A U. Breithauer , E. Horneber  
**Proceedings of the conference with EURO-VHDL'96 and exhibition on European Design Automation** September 1996

8 Gate-level simulation of digital circuits using multi-valued Boolean algebras 77%  
A Scott Woods , Giorgio Casinovi  
**Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**  
December 1995

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